AMENDMENT TO SPECIFICATION

A marked-up copy of the changes to selected paragraph(s) is provided below. Please enter these changes to the specification in the record.

Please delete paragraph [0046] as follows:

~~Figure 26 shows a representation of conductivity fill shapes for improved ESD robustness in accordance with the invention;~~

Please amend paragraph [0047] as follows:

Figure ~~27~~ 26 shows a representation of a cheesing feature for improved ESD robustness in accordance with the invention;

Please amend paragraph [0048] as follows:

Figure ~~28~~ 27 shows a flowchart implementing a method for verifying the connection between the pad and the ESD network in accordance with the invention;

Please amend paragraph [0049] as follows:

Figure ~~29~~ 28 shows a representation of an ESD Interconnect Translation Box in accordance with the invention; and

Please amend paragraph [0050] as follows:

Figure ~~30a~~ 29a and ~~30b~~ 29b show flowcharts implementing a method for allowing for calculation of the ESD robustness in accordance with the invention.

Please amend paragraph [0119] as follows:

7. Account for surrounding fill shapes. ~~(See, Figure 26.)~~

Please amend paragraph [0120] as follows:

8. Account and adjust for "cheesing" (removal of interconnect material inside the interconnect) of the interconnect. (See, Figure ~~27~~ 26.)

Please amend paragraph [0124] as follows:

In this "ESD Interconnect" hierarchical p-cell, item (1) is achieved by the flow of Figure ~~28~~ 27. At step 2800, the flow of the invention establishes the interconnection path of the pad level. At step 2805, the flow verifies an ESD interconnect at that level. At step 2810, the flow verifies a ESD via at the level below. The flow at step 2810 is repeated until the lowest level connects to highest metal design level of the input of the ESD network of the corresponding ESD device to that pad. The "ESD Interconnect" can be a single p-cell which contains multiple levels of metal from pad X to ESD p-cell Y where the system verifies the connectivity.

Please amend paragraph [0126] as follows:

For item (3), the checking and verification of the correct wire width and via number is never below the ESD robustness level of the circuit can be verified using the

information of the inherited parameters contained on the translation box (Figure ~~29~~ 28) formed around the electrical schematic of the hierarchical parameterized cell. The electrical schematic translation box contains the circuit type, the inherited parameters, and pin connections. The translation box may also contain functions 29, including for example, ballasting, fill and cheese. The translation box will allow the transformation of the schematic to the graphical and vice versa. From this, the ESD robustness of the circuit can be determined and stored in the circuit from electrical measurement tables of the design system, as discussed below. Also, from this, the verification that the ESD Interconnect structure p-cell is more ESD robust can be calculated from the ESD robustness wire calculations. The ESD robustness can be addressed based on the knowledge of items (6), item (7) and item (8).

Please amend paragraph [0135] as follows:

Figure ~~30a~~ 29a shows a flow for using the lookup table as discussed above. At step 3005, the ESD Failure Model (HBM, MM, CDM, Other) is defined. At step 3010, the ESD desired failure level is defined. At step 3015, the Technology File Data and Level Information (Insulators, Metal Thickness) is placed in the system. At step 3020, the fill requirements for that level are defined. At step 3025, the cheese requirements are defined. At step 3030, the metal linewidth is calculated. At step 3035, the ballast requirements are defined.

Please amend paragraph [0136] as follows:

Figure ~~30b~~ 29b shows a flow chart based on an analytical model. At step 3050, the ESD pulsewidth is defined. At step 3055, the Electrothermal Model is defined (e.g., Wunsch-Bell, Smith-Littau, Pierce, Voldman). At step 3060, the desired ESD failure rate is defined. At step 3065, the Technology File Data and Level Information (Insulators, Metal Thicknesses) is placed within the system. At step 3070, the fill requirements for that level are defined. At step

3075, the cheese fill requirements are defined. At step 3080, the Metal Linewidth is calculated from the Electrothermal Model. At step 3085, the ballasting requirements are defined.

Please amend paragraph [0138] as follows:

If the ESD network translation (Figure ~~29~~ 28) box contains information that ESD ballasting is required for that specific design, the check then verifies that the ESD interconnect also contains this requirement or design failure is stated. Hence, an ESD Interconnect p-cell can have as a parameter the formation of a plurality of interconnects, and also verifies that this feature is "checked" relative to the ESD network translation box information of the ESD p-cell for the highest level of the p-cell and the lowest level of the ESD Interconnect p-cell.

REPLACEMENT DRAWINGS

IN THE DRAWINGS:

Attached hereto are replacement drawings for figures 27-30b (now figures 26-29b), without any markings. The changes to the drawings are explained below, in the "REMARKS" section. All of the drawings on the replacement sheet, as originally filed, are provided herein. The header of each revised drawing sheet includes the following information: (i) "Replacement Sheet", (ii) application number and (iii) date information. The Examiner is requested to provide an indication of such consideration in the next Office Action.